

AMENDMENTS TO THE CLAIMS

Claims 1-10 (canceled)

- 5 Claim 11 (Previously Presented): A delay lock circuit for generating a second clock according to a first clock and synchronizing the first clock and the second clock, the delay lock circuit comprising:
- a comparator for determining if corresponding periods of the first clock
and the second clock are synchronized and generating a
10 corresponding comparison signal;
- a delayer electrically connected to the comparator for delaying the first clock so as to change a delay time between the corresponding periods of the first clock and the second clock; and
- a controller to control the delay lock circuit;
- 15 wherein the controller uses the delayer to perform a correcting process to increase or decrease the delay time between the corresponding periods of the first clock and the second clock by a correction interval, wherein a subsequent correction interval of a subsequent correcting process is less than a previous correction interval of a previous
20 correcting process, and the controller terminates the correcting process if the correction interval is smaller than a predetermined value.

- Claim 12 (Previously Presented): The delay lock circuit of claim 11, wherein the delayer comprises a plurality of delay units, each of the
25 delay units capable of increasing the delay time between the corresponding periods of the first clock and the second clock by a unit delay time.

- Claim 13 (Previously Presented): The delay lock circuit of claim 11,
30 wherein the delay lock circuit further comprises a register to store information about the correction interval.

Claim 14 (Previously Presented): The delay lock circuit of claim 11, wherein the comparator compares the time interval between a period of the second clock and a corresponding reference period of the first clock to generate the comparison signal, wherein the period of the first clock
5 corresponding to the period of the second clock leads the reference clock by a predetermined reference interval.

Claim 15 (canceled)

10 Claim 16 (Previously Presented): A method for performing a delay lock to generate a second clock according to a first clock and to synchronize the second clock with the first clock, the method comprising:
executing a plurality of correcting processes, each of which increases or
decreases by a respective correction interval a respective delay
15 time between corresponding periods of the first clock and the second clock; and
terminating the plurality of correcting processes when the correction interval is smaller than a predetermined value;
wherein a subsequent correction interval for a subsequent correcting
20 process is less than a previous correction interval of a previous correcting process.

Claim 17 (Previously Presented): The method of claim 16, wherein the correcting process further comprises:
25 determining if the first clock and the second clock are synchronized and generating a corresponding comparison result;
wherein the delay time between the corresponding periods of the first clock and the second clock for the subsequent correcting process is increased or decreased by the subsequent correction interval according
30 to the comparison result.

Claim 18 (Previously Presented): The method of claim 17, wherein

determining if the corresponding periods of the first clock and the second clock are synchronized is decided by comparing the time interval between a period of the second clock and a corresponding reference period of the first clock.

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Claim 19 (Previously Presented): The method of claim 17 further comprising:

prior to the plurality of correcting processes, setting the correction interval to a predetermined initial value.

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Claim 20 (Previously Presented): The method of claim 17, wherein the method is used for a delay lock circuit, the delay lock circuit comprising:

a delayer for delaying the first clock in order to change the delay time

15 between the corresponding periods of the second clock and the first clock;

wherein when the delay time between the corresponding periods of the first clock and the second clock is increased or decreased by the correction interval, the delayer is used to delay the second clock so that

20 the delay time between the corresponding periods of the first clock and the second clock is modified.

Claim 21 (Previously Presented): The method of claim 20, wherein the delayer comprises a plurality of delay units, each of the delay units
25 capable of increasing the delay time between the corresponding periods of the first clock and the second clock by a unit delay time.

Claim 22 (Previously Presented): The method of claim 20, wherein the delay lock circuit further comprises a comparator electrically connected
30 to the delayer for determining if the corresponding periods of the first clock and the second clock are synchronized and generating a corresponding comparison result; wherein the delay time between the

corresponding periods of the first clock and the second clock is increased or decreased by the correction interval according to the comparison result.

- 5 Claim 23 (Previously Presented): The method of claim 22, wherein the comparator compares the time interval between a period of the first clock and a corresponding reference period of the second clock to generate the comparison result; wherein the period of the first clock corresponding to the period of the second period leads the reference
10 period by a predetermined reference interval.

Claim 24 (Previously Presented): The method of claim 20, wherein the delay lock circuit further comprises a register to store information about the correction interval.

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